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*	В	US-6,625,572 B1	09-2003	Zemlyak et al.	703/19
*	С	US-6,230,114 B1	05-2001	Hellestrand et al.	703/13
*	D	US-6,052,524 A	04-2000	Pauna, Mark R.	703/22
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*	F	US-5,991,533	11-1999	Sano et al.	703/28
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	N	EP 0 772 140 A <b>1</b>	05-1997	BE	Karl Van Rompaey et al.	G06F 17/50
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	U	Hopes T. "Hardware/software co-verification, an IP vendors Viewpoint" Computer Design: VLSI in Computers and Processors, 1998. ICCD 98' Proceedings, 10/07/1998, pages 1-5.			
	٧	Arnold S. Berger, "Applying Hardware/Software Co-Design to Systems-on-a-Chip", IEEE 1998, pages 22-28.			
	w	Guerra L., Fitzner J., Talukdar D., Schlager C., Tabbara B., Zivojnovic V., "Cycle and Phase Accurate DSP Modeling and Integration for HW/SW Co-Verification" ACM 1999, pages 964-969.			
	х	Smith C., Frank G., Cuadrado J. "An Architechure Design and Assessment System for Software/Hardware Codesign" IEEE 1985, pages 417-424.			

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.